Series Compensator Based on Cascaded Transformers Coupled With Three-Phase Bridge Converters

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***Abstract*—This paper proposes a multilevel series compensator (MSC) to deal with voltage sags/swells, harmonic compensation, or reactive power compensation. Such a device can be considered as a dynamic voltage restorer or a series active power filter (Series-APF). The MSC can improve the power quality of loads located in stiff systems. The configuration is based on three-phase bridge (TPB) converters connected by means of cascaded single-phase transformers. This arrangement permits the use of a single dc-link. A generalization for K-stages in which K-transformers are coupled with K-TPB converters is presented. The topology permits generating a high number of levels in the voltage waveforms with a low number of power switches in comparison with a classic topology. The multilevel waveforms are generated by the converters through a suitable pulsewidth modulation (PWM) strategy that takes into consideration the transformer turns ratios. Modularity and simple maintenance make the proposed MSC an attractive solution compared with some conventional configurations. Model, PWM strategy, and overall control are discussed in this paper. Simulation and experimental results are presented as well.**

***Index Terms*—Cascaded transformers, dynamic voltage restorer, multilevel series compensator, pulse-width modulation, series active power filter.**

I. Introduction

DISTRIBUTION power systems are suffering hard impact in their power quality. This is due to the intensive use of nonlinear loads added with the growth of renewable energy sources. Such aspects have been leading electrical power system to poor power quality levels. Most common disturbances include: 1) harmonic voltages/currents; 2) voltages imbalances; 3) voltage sags/swells; 4) flickers; 5) transients; and 6) interruptions.

Among them, voltage sags have been considered the most important power quality problem and have been attracting much attention in the literature [1]–[3]. To mitigate voltage disturbances at the grid, some custom power devices have been introduced and investigated. For instance, dynamic voltage restorer (DVR) [4], [5], series active power filter (Series-APF) [6], [7], and unified power quality conditioner (UPQC) [8], [9]. These three options satisfy the series voltage compensation criteria. However, each of them present particularities on their application field. UPQC is attractive to compensate both voltage and current disturbances by using series and shunt converters [10]. If the dc energy storage unit is not a critical issue for the compensator design, DVRs should be suitable due to short time operation feature [11]. On the other hand, Series-APF can operate without a dc source connected in the dc-link for harmonic voltages compensations. In this case, the dc-link regulation strategy must be considered for a satisfactory operation [11], [12].

The series compensator (DVR or Series-APF) is commonly composed of the following: 1) injection transformers; 2) voltage source converter (VSC); 3) energy storage; 4) optional passive filters; and 5) protection circuits (e.g., bypass thyristors).

The VSC-based on two-level (2L) topology is the most common solution used for low-voltage systems [4], [13]. However, for high-voltage levels (i.e., high-power applications), 2L-based converters have experienced limitations and difficulty to penetrate in this market [14]. The cost associated for designing a 2L-based compensator for more than 690 V_{rms} (according to IEC) makes this solution not feasible for high-voltage applications [13], [14]. In this context, the multilevel-based VSC technology has become the most mature and feasible solution for this type of applications [4]. Multilevel series compensators (MSCs) have been investigated in different aspects [13], [15]–[19], which make clear the fact that the multilevel converters ensure that voltage waveforms can be synthesized with lower harmonic content than 2L converters and also operate at a higher dc voltage [19].

Some multilevel configurations can be highlighted from the technical literature [4], [19]–[21]. However, those configurations have some issues associated to the high number of dc-link capacitors, inherent in their topology. For instance, cascaded neutral point-clamped (NPC) and cascaded flying capacitor topologies have issues with unbalanced dc-link voltages and power sharing in each cell [22]. In addition, the lifetime of

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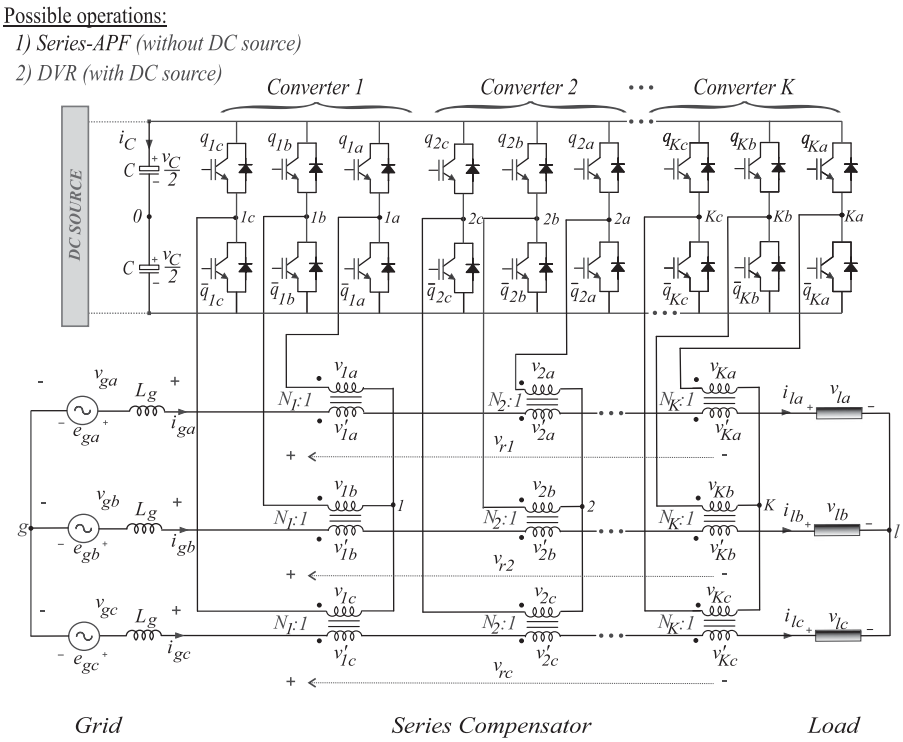

Fig. 1. Proposed MSC. Generalization with K-stages (i.e., K-cascaded transformers and K-TPB converters).

dc-link capacitors stands out as one of the most important issues in terms of failure rate at the operation of power electronic systems [23]–[25]. Then, a high number of dc-link capacitors increases the failure probability of the topology.

To cope with this issue, the concept of using cascaded transformers has been introduced as an alternative solution [26]–[28]. In this way, the multilevel features can be guaranteed by using a single dc-link capacitor. A conventional DVR based on cascaded transformer coupled with H-bridge (HB) converters was presented in [4]. Usually, injection transformers are taken into consideration for the series voltage compensator design [29]. In this way, the transformer turn ratio associated with each transformer can be considered to improve the waveform quality of the output voltage generated by the compensator. This paper proposes a series compensator based on cascaded transformers coupled with three-phase bridge (TPB) converters [30], as illustrated in Fig. 1. Equivalent multilevel operation is achieved with reduced number of semiconductor devices in comparison with conventional HB. The multilevel waveforms are generated by TPB converters through a suitable pulsewidth modulation (PWM) strategy associated with the transformer turns ratio. The modularity and simple maintenance make the proposed MSC an attractive solution in comparison with some conventional configurations. The model and control are addressed in this paper. Simulation and experimental results are presented too.

II. Proposed MSC Model

The configuration depicted in Fig. 1 is generalized for K-stages (i.e., K-transformers and K-TPB converters). The converters legs are represented by K-power switches (i.e., q_{1j}, $\overline{q}_{1j}$, q_{2j}, $\overline{q}_{2j}$, …, q_{Kj}, and $\overline{q}_{Kj}$) in which the subscript j is related to each phase ($j = a, b, c$). In addition, power switches q and $\overline{q}$ are complementary from each other. The switching states of all power switches are represented by binary variables, where $q = 1$ indicates a closed switch while $q = 0$ an open one.

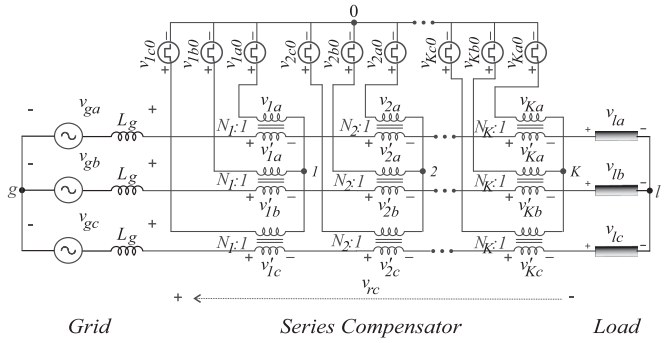

Fig. 2. Ideal equivalent circuit for generalization of the proposed MSC.

The configuration model becomes simple when its ideal equivalent circuit, see Fig. 2, is considered. In this way, the converter pole voltages ($v_{1j0}, v_{2j0}, \ldots, v_{Kj0}$), can be expressed as

$$v_{kj0} = (2q_{kj} - 1)\frac{v_C}{2} \tag{1}$$

where k corresponds to each stage (i.e., $k = 1, 2, 3, \ldots, K$) and v_C is the dc-link voltage.

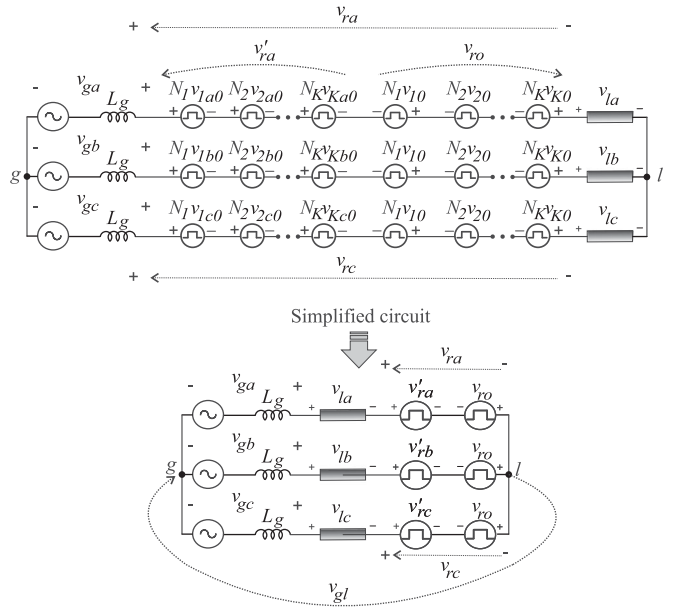

Fig. 3. Equivalent simplified circuit. Modified (on the top). Simplified (on the bottom).

The voltages at the primary side of the injection transformers for each phase are expressed as

$$v_{ka} = v_{ka0} - v_{k0} \tag{2}$$

$$v_{kb} = v_{kb0} - v_{k0} \tag{3}$$

$$v_{kc} = v_{kc0} - v_{k0}. \tag{4}$$

The system model considering the grid voltages (v_{gj}), transformer voltages at the secondary side ($v_{1j}^{'}$, $v_{2j}^{'}, \ldots, v_{Kj}^{'}$) and load voltages ($v_{lj}$) can be expressed as

$$v_{gj} = (v_{1j}^{'} + v_{2j}^{'} + \cdots + v_{Kj}^{'}) + v_{lj} - v_{gl} \tag{5}$$

where $v_{1j}^{'} = N_1(v_{1j0} - v_{10})$, $v_{2j}^{'} = N_2(v_{2j0} - v_{20}), \ldots, v_{Kj}^{'} = N_K(v_{Kj0} - v_{K0})$ in which N_1, $N_2, \ldots, N_K$ are the transformer turns ratios associated with converters 1, 2,..., K, respectively.

A simplified circuit can be obtained from the circuit depicted in Fig. 2 by considering perfect isolation from primary to secondary side of the transformers (i.e., ideal transformers), as shown in Fig. 3. Such an equivalent circuit permits to clarify the approach used to write the following equations. It should be noticed that the output voltages (v_{rj}) of the resultant converter can be expressed as

$$v_{rj} = v_{rj}^{'} - v_{ro} \tag{6}$$

$$v_{rj}^{'} = N_1 v_{1j0} + N_2 v_{2j0} + \cdots + N_K v_{Kj0} \tag{7}$$

$$v_{ro} = N_1 v_{10} + N_2 v_{20} + \cdots + N_K v_{K0}. \tag{8}$$

From (8) and (5) the system model is simplified as

$$v_{gj} - v_{lj} = v_{rj}^{''} = v_{rj}^{'} - v_{ro} - v_{gl}. \tag{9}$$

Voltages v_{rj} can have a maximized number of levels if the voltages ($v_{rj}^{'}$) assume a suitable sequence of the switching states. This is achieved by considering the transformer turns ratios ($N_1, N_2, \ldots, N_K$). Table I shows a particular case with three transformers per phase and three TPB converters, in which the voltage $v_{rj}^{'}$ can reach eight different levels per phase according to the switching states. In this case, the compensator must operate with different transformer turns ratios (e.g., $N_k = 2^{(k-1)}$). It can be seen that these ratios provide the best (higher) number of voltage levels, symmetrically spaced from each other. Fig. 4 presents an one-dimension region of output voltage $v_{rj}^{'}$ for each phase (e.g., $j = a, b, c$) associated with switching states [q_{1j}, q_{2j}, and q_{3j}]. Such a representation permits to easily synthesize the reference output voltage by always using the switching states nearest to the reference output voltage. This approach is similar to that one presented in [31] and has advantages of reducing the switching losses of the converter topology. It is worth noting that either the order of the stages or transformers polarity can be modified to change the rated switching frequency in the legs with higher voltage or higher current.

Table II shows the generalization for K-transformers and K-TPB converters. The respective levels disposition in one-dimension region is presented in Fig. 5. Notice that the

TABLE I
VARIABLES FOR RESULTANT CONVERTER WITH THREE CASCADED TRANSFORMERS PER PHASE AND THREE TPB CONVERTERS IN WHICH $N_1 = 1$, $N_2 = 2$, AND $N_3 = 4$

State	Leg state			Output voltage
	q_{3j}	q_{2j}	q_{1j}	$v_{rj}^{'}=N_1 v_{1j0}+N_2 v_{2j0}+N_3 v_{3j0}$
-7	0	0	0	$-7v_C/2$
-5	0	0	1	$-5v_C/2$
-3	0	1	0	$-3v_C/2$
-1	0	1	1	$-v_C/2$
1	1	0	0	$v_C/2$
3	1	0	1	$3v_C/2$
5	1	1	0	$5v_C/2$
7	1	1	1	$7v_C/2$

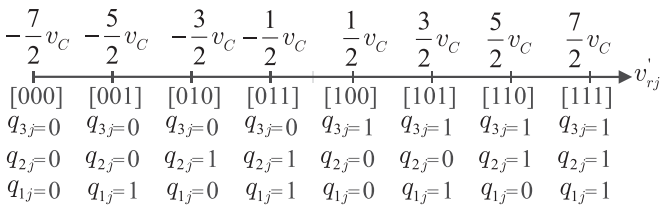

Fig. 4. One-dimension of output voltage ($v_{rj}^{'}$) levels region for three-stages (i.e., $K = 3$ that means $N_1 = 1$, $N_2 = 2$, and $N_3 = 4$).

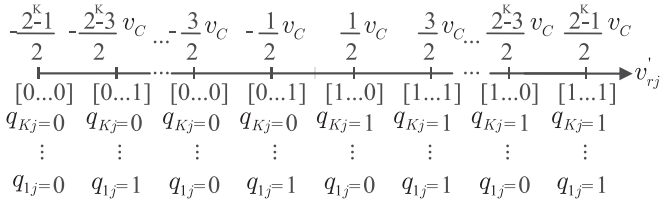

Fig. 5. One-dimension of output voltage ($v_{rj}^{'}$) levels region for K-stages (i.e., that means $N_1 = 1$, $N_2 = 2$, $N_3 = 4, \ldots, N_K = 2^{(K-1)}$).

TABLE II
VARIABLES FOR RESULTANT CONVERTER WITH K-CASCADED TRANSFORMERS PER PHASE AND K-TPB CONVERTERS WITH $N_K = 2^{(K-1)}$, VALID FOR $K \geq 3$

State	Leg state			Output voltage
	q_{Kj}	...	q_{1j}	v'_{rj}=$N_1 v_{1j0}$+$N_2 v_{2j0}$ +...+ $N_K v_{Kj0}$
-(2^K-1)	0	...	0	-$(2^K-1)v_C/2$
-(2^K-3)	0	...	1	-$(2^K-3)v_C/2$
-(2^K-5)	0	...	0	-$(2^K-5)v_C/2$
⋮	⋮	⋯	⋮	⋮
-1	0	...	1	-$v_C/2$
1	1	...	0	$v_C/2$
⋮	⋮	...	⋮	⋮
2^K-5	1	...	1	$(2^K-5)v_C/2$
2^K-3	1	...	0	$(2^K-3)v_C/2$
2^K-1	1	...	1	$(2^K-1)v_C/2$

transformer turn ratios follow a geometric sequence with ratio equal to 2 (e.g., $N_1 = 1$, $N_2 = 2$, $N_3 = 4$, $N_4 = 8$, $N_5 = 16, \ldots$, $N_K = 2^{(K-1)}$) resulting always in the best option in terms of maximum number of levels generated at the voltage v'_{rj} and symmetrical dv/dt at v_{rj} from one level to the other.

It should be noted that, in this case, there is no redundant levels and the switching states present a maximized number of different levels (i.e., 2^K). If the redundancy is a priority, at least one of the transformer turns ratios must be equal. For instance, $N_1 = 1$ and the others $N_2 = N_3 = \cdots = N_{(K-1)} = N_K = 2^{(K-1)}$.

III. PWM STRATEGY

The pulsewidth modulation (PWM) technique used in this work is the level-shifted-carrier-based PWM (LSPWM). Differently from conventional nonsinusoidal carrier-based PWM (CPWM), a simpler algorithm calculation can be obtained. It takes into consideration references for the resultant output voltage (v^{*}_{rj}).

Considering that a voltage controller provides references for the resultant converter ($v^{*''}_{rj} = (v_{gj} - v_{lj})^{*}$), the references $v^{*'}_{rj}$ become

$$v^{*'}_{rj} = v^{*''}_{rj} + v^{*}_{rogl} \tag{10}$$

where $v^{*'}_{rj} = v^{*'}_{1j} + v^{*'}_{2j} + \cdots + v^{*'}_{Kj}$ and v^{*}_{rogl} is a degree of freedom from the system characteristics.

The reference voltage for v^{*}_{rogl} is calculated as

$$v^{*}_{rogl} = \mu^{*}_{rogl} v^{*}_{rogl\,\max} + (1 - \mu^{*}_{rogl}) v^{*}_{rogl\,\min} \tag{11}$$

where $0 \leq \mu_{rogl} \leq 1$ and

$$v^{*}_{rogl\,\min} = -0.5 v^{*}_{C}(N_1 + \cdots + N_K) - \min\{v^{*''}_{rj}\} \tag{12}$$

$$v^{*}_{rogl\,\max} = 0.5 v^{*}_{C}(N_1 + \cdots + N_K) - \max\{v^{*''}_{rj}\}. \tag{13}$$

In this way, once voltages $v^{*''}_{rj}$ (i.e., $v^{*''}_{r1}$, $v^{*''}_{r2}$, and $v^{*''}_{r3}$) are given from the controller, the algorithm to calculate $v^{*'}_{rj}$ is summarized in following steps.

1) Calculate the $v^{*}_{rogl\,\min}$ and $v^{*}_{rogl\,\max}$ values according to (12) and (13).

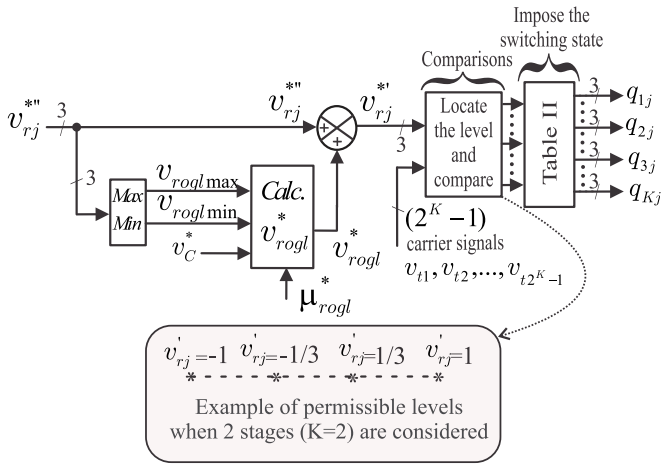

Fig. 6. PWM block diagram of generalized proposed MSC. Example of permissible levels were normalized by $v_C/2$.

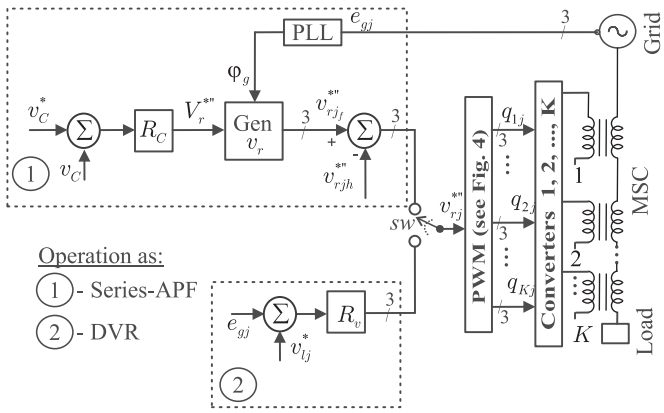

Fig. 7. Control block diagram of proposed MSC. Possible operations as a Series-APF (option 1) or as a DVR (option 2).

2) Choose μ^{*}_{rogl} between 0 and 1.
3) Determine v^{*}_{rogl} from (11).
4) Calculate $v^{*'}_{rj}$ from (10).

In this way, the reference voltages $v^{*'}_{rj}$ are compared with $2^n - 1$ triangular waveforms, which are level-shifted carriers (v_{t1} to v_{t2^n-1}) placed according to the levels shown previously in Table II. The result of this comparison gives the switching states ($q_{1j}, q_{2j}, \ldots, q_{Kj}$) that are imposed to each TPB converter. Fig. 6 summarizes each step of this PWM strategy.

IV. CONTROL STRATEGY

Fig. 7 shows the control strategy of the proposed MSC. Notice that there are two options of operation: 1) as a harmonic Series-APF; or 2) as DVR. The first option regulates the dc-link voltage v_C by means of a conventional proportional-integral (PI) controller. Such a controller is represented by the block R_C which provides a small amplitude reference of the resultant voltage to be compensated ($V^{*''}_{r}$). The block Gen $- v_r$ generates small reference voltages $v^{*''}_{rjf}$ (at the fundamental frequency) synchronized with e_{gj} through the phase-locked-loop (PLL).

These small signals are subtracted from the harmonic voltage signals $v_{rjh}^{*''}$ to be compensated providing the voltages $v_{rj}^{*''}$. More details about this control approach can be observed in [7]. In the second option, there is only controller R_v whose input signals are the grid voltages (v_{gj}) and reference load voltages v_{lj}. The output of controller R_v gives reference voltages $v_{rj}^{*''}$ for the PWM strategy. As shown in Fig. 7, the switch SW indicates the selection of Series-APF or DVR operation.

V. Comparisons and Analysis

A. Number of Levels per Power Switch

This feature gives an idea of the cost-benefit associated with the studied topology. Assuming that the number of power switches are the same for both the proposed MSC and conventional HB converters [4] configurations (i.e., four power switches per phase), the proposed MSC has $K = 2$ with transformer turns ratios $N_1 = 1$ and $N_2 = 2$ while the conventional HB has $N_1 = 1$. Thus, the number of levels generated at $v_{rj}^{'}$ per phase with proposed configuration is 4 ($3v_C/2$, $v_C/6$, $-v_C/6$, and $-3v_C/2$) whereas the conventional HB provides three levels (v_C, 0 and $-v_C$). Then, taking into consideration the number of levels divided by the number of power switches used, the following comparison can be noted:

- Proposed MSC, number of levels per power switches: $\frac{4}{4} = 1.00$;
- Conventional HB [4], number of levels per power switches: $\frac{3}{4} = 0.75$

Considering eight power switches per phase, the proposed MSC has $K = 4$ with transformer turns ratios equal to $N_1 = 1$, $N_2 = 2$, $N_3 = 4$, and $N_4 = 8$. The conventional HB has a maximized number of level with transformer turns ratios equal to $N_1 = 1$, $N_2 = 3$. Then, the number of levels that can be generated at the output voltage $v_{rj}^{'}$ in each phase is 16 for proposed MSC and 9 for conventional HB. Then, by dividing this by the number of power switches, it is possible to derive that:

- Proposed MSC, number of levels per power switches: $\frac{16}{8} = 2.00$;
- Conventional HB [4], number of levels per power switches: $\frac{9}{8} = 1.13$

It can be seen that proposed configuration presents a better performance if compared to conventional with HB, considering this characteristic. Hence, such an improvement is close to 33% (1/0.75) in the first case (with four power switches), while the second case (with eight power switches) is 76.99% (2/1.13). In this way, this feature (i.e., the improvement) increases with the raise of power switches considered for the configurations. Although the proposed MSC requires more transformers, they have smaller rated power than those used in conventional HB topology.

B. Topological Comparison

A topological comparison between proposed MSC (TPB) and the conventional HB is presented in Table III. It can be seen that proposed MSC has lower number of power switches in comparison with conventional one.

TABLE III
Device Count Comparison With the Same Number of Stages (K)

Main devices	Conventional HB [4]	Proposed TPB
Transformers	$3K$	$3K$
IGBTs	$12K$	$6K$
Capacitors	1	1
Levels/phase	3^K	2^K

TABLE IV
WTHD for Proposed MSC and Respective Transformer Turns Ratio for K=1, 2, and 3

Proposed MSC	Transformer turns ratios	WTHD (%)
1 stage ($K = 1$)	1:1 ($N_1 = 1$)	0.200
2 stages ($K = 2$)	1:1 ($N_1 = 1$) 2:1 ($N_2 = 2$)	0.055
3 stages ($K = 3$)	1:1 ($N_1 = 1$) 2:1 ($N_2 = 2$) 4:1 ($N_3 = 4$)	0.023

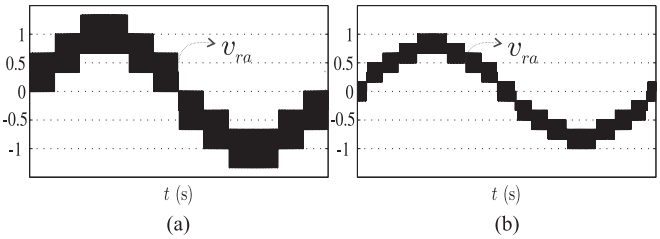

Fig. 8. Simulation results. Resultant phase-voltage (v_{ra}) in phase a in which proposed MSC has two TPB converters. (a) Transformer turns ratios being equal to $N_1 = N_2 = 1$. (b) Transformer turns ratios being equal to $N_1 = 1$ and $N_2 = 2$.

C. Harmonic Distortion Evaluation

The weighted total harmonic distortion (WTHD) of the resultant voltages (v_{rj}) in the proposed MSC has been computed by using

$$\text{WTHD}(p) = \frac{100}{a_1}\sqrt{\sum_{i=2}^{p}\left(\frac{a_i}{i}\right)^2} \tag{14}$$

where a_1 is the amplitude of the fundamental voltage, a_i is the amplitude of i-th harmonic and p is the number of harmonics taken into consideration.

Then, considering a maximum injection of v_{rj} and a balanced system, the WTHD of the voltages v_{rj} for proposed configuration can be observed in Table IV. In this result, the switching frequency (f_s) was fixed in 10 kHz. The number of stages defines how many transformers and three-phase converters are used per phase. For example, by using two stages, that proposed MSC operates with two transformers and two TPB converters in each phase.

It can be seen in Table IV that, as expected, the WTHD value decreased with the increase of the number of stages used in proposed MSC. The waveforms for that result, with two and three stages, are shown in Figs. 8 and 9, respectively. It can

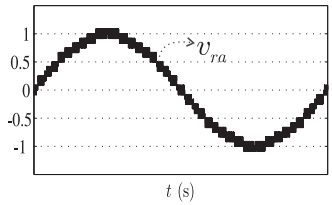

Fig. 9. Simulation results. Resultant phase-voltage (v_{ra}) in phase a when proposed MSC has three TPB converters. Transformer turns ratios being equal to $N_1 = 1$, $N_2 = 2$, and $N_3 = 4$.

TABLE V
LOSSES COMPARISON BETWEEN THE PROPOSED MSC OPERATING WITH TWO STAGES ($N_1 = 1$ AND $N_2 = 2$) AND THE CONVENTIONAL HB WITH 1 STAGE

Case I: $P_{load} = 40$ kW.				
Configuration		**Semiconductor Losses Estimation**		
Topology	**Stages**	**Switching**	**Conduction**	**Total**
Conventional HB	1	0.73 kW	0.25 kW	0.98 kW
Proposed TPB	2	0.44 kW	0.19 kW	0.63 kW
Prop./Conv.	2	60.3 %	76 %	64.3 %
Case II: $P_{load} = 275$ kW.				
Configuration		**Semiconductor Losses Estimation**		
Topology	**Stages**	**Switching**	**Conduction**	**Total**
Conventional HB	1	4.5 kW	0.73 kW	5.23 kW
Proposed TPB	2	2.6 kW	0.52 kW	3.12 kW
Prop./Conv.	2	57.8 %	71.23 %	59.7 %

be seen that the proposed MSC operating with $K = 2$ has presented a WTHD reduction close to 72.5% in comparison with MSC operating with $K = 1$ (i.e., which lies in a conventional three-phase compensator). Additionally, for MSC operation with $K = 3$, the reduction achieved 88.5% compared to the conventional (i.e., a single TPB converter).

D. Semiconductor Losses Estimation

Thermal module, an existing tool in power simulator (PSIM) v 9.0, was considered in order to have an indicative that could permit to compare semiconductor losses estimation between proposed and conventional topologies. This aims to indicate an acceptable figure of merit to reflect how far semiconductor losses of proposed MSC are faced to losses estimated of conventional one. Such a tool was used with calibration parameters that gives an equivalent loss estimation compared to the conventional method to estimate losses in [32] that was obtained through regression model, achieved by experimental tests. The power switch losses model includes the following: 1) insulated gate bipolar transistor (IGBT) and diode conduction losses; 2) IGBT turn-ON losses; 3) IGBT turn-OFF losses; and 4) Diode turn-OFF energy.

Table V shows a comparison between the conventional HB converter [4] and the proposed MSC that uses TPB converter for two different cases of load power (e.g., 40 and 275 kW). Additionally, it was considered the same number of power switches (i.e., six IGBTs) for both configurations. Additionally, the same WTHD (e.g., 0.21%) value was imposed to both of them. This was achieved by fixing the WTHD in 0.21% for conventional configuration that was obtained with sampling frequency

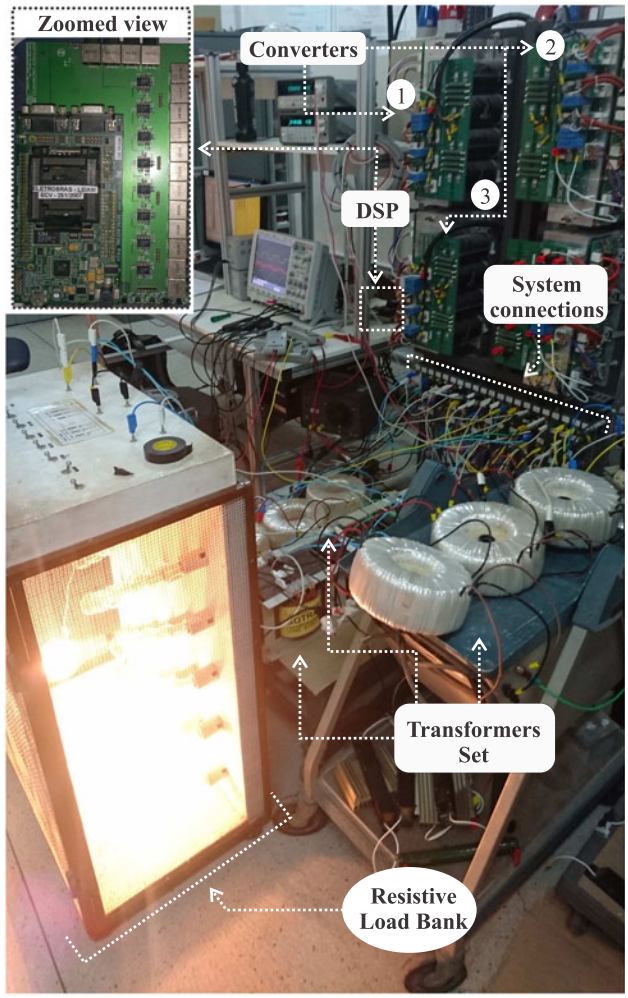

Fig. 10. Photograph of the implemented prototype for experimental tests.

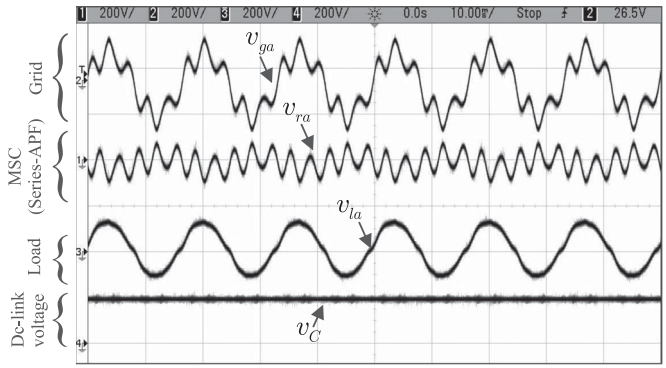

Fig. 11. Experimental result. MSC operating as a series-APF. System voltages and the regulated dc-link voltage.

equal to 7.5 kHz. To obtain the same WTHD value, proposed configuration was operated with a frequency decreased up to 3.3 kHz. Such a reduction can be observed via switching losses estimation.

The normalized results of proposed topology in comparison with the conventional one are presented in Table V. It can be

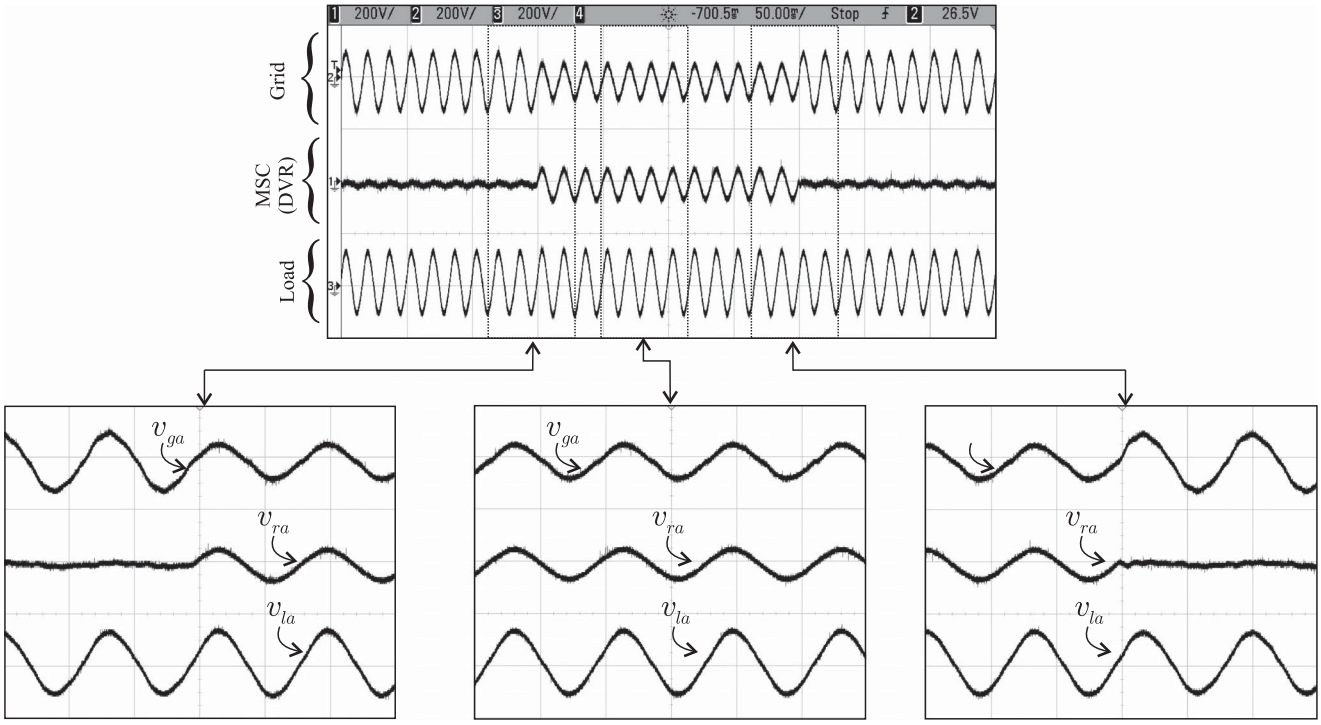

Fig. 12. Experimental result. MSC operating as a DVR. System voltages.

seen that, for this scenarios of application, that reduction will be more significant for switching losses estimation than conduction losses. Therefore, depending on the power level of application, the proposed MSC can operate with lower losses if compared to the conventional one. The total losses reduction was close to 40% and the reduction was higher for the highest load power. It is possible that such reduction can compensate the losses provided by an additional transformer (per phase), that would be needed for the proposed MSC with two stages.

VI. Simulation Results

Simulation results obtained from PSIM $v9.0$ are shown in Figs. 8 and 9. Such outcomes show resultant voltage of the converter (v_{ra}), in one phase (i.e., phase-a), with PWM implementation accordingly to the PWM strategy presented earlier. Fig. 8(a) and (b) considers only converters 1 and 2 with two single-phase transformers connected in each phase. It can be seen that the result presented in Fig. 8(a) is equivalent to that obtained with 3L-NPC converter or cascaded HB with equal dc-link voltages. Fig. 9 shows implementation with converters 1, 2, and 3 as well as transformers turns ratio equal to $N_1 = 1$, $N_2 = 2$, and $N_3 = 4$. Results for the other phases are similar.

VII. Experimental Results

The proposed MSC studies were validated with some experimental tests in a downscaled prototype, as observed in Fig. 10. The main components of experimental setup are converters composed by IGBTs from Semikron SKM50GB123D with drivers SKHI23 that are linked with the control strategy by means of a digital signal processor (DSP) TMS320F28335 programmed via microcomputer. DSP board has interface connections to send gate signals via optical fiber cables whereas measurement were accomplished with dedicated sensors boards connected via coaxial cables to analog/digital DSP inputs. The dc-link capacitor considered for the setup was $C = 2200\ \mu$F and the switching frequency for the power switches was considered as $f_{\text{sw}} = 10$ kHz.

The dynamic operation of the MSC operating as a Series-APF and as a DVR has been verified. The implementation for this dynamic operation considering two options of operation (i.e., as a series-APF or as a DVR) was made through an equivalent single-phase configuration. In order to filter the high-frequency components provided by PWM converter, filtering capacitor and inductors (i.e., passive LCL filter) were connected in parallel with the transformers.

Fig. 11 shows a steady state result in which the MSC is operating as a Series-APF. In this case, a fifth harmonic voltage was added in the fundamental voltage at the grid (i.e., $v_{ga} = V_g \sin(w_g t) + 0.2 V_g \sin(5 w_g t)$). The dc-link voltage ($v_C$) was regulated considering the control strategy described previously. It can be seen that disturbance is well compensated by the converter voltage (v_{ra}). The load voltage waveform (v_{la}) was virtually sinusoidal.

Fig. 12 shows MSC acting as a DVR. The compensator was tested under a voltage sag. It can be seen that the voltage sag was compensated satisfactorily. To guarantee that the injected voltage was in phase with the grid, a PLL based on fictitious electrical power (i.e., power-based PLL) was considered. More details of this PLL can be found in [33].

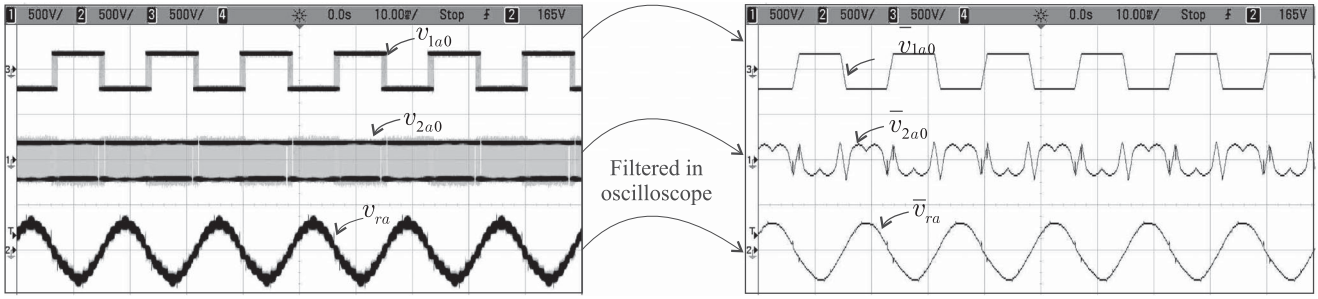

Fig. 13. PWM converter voltages in phase a. The PWM implementation of proposed MSC uses two converters (1 and 2) and two transformers per phase with $N_1 = 1$ and $N_2 = 2$.

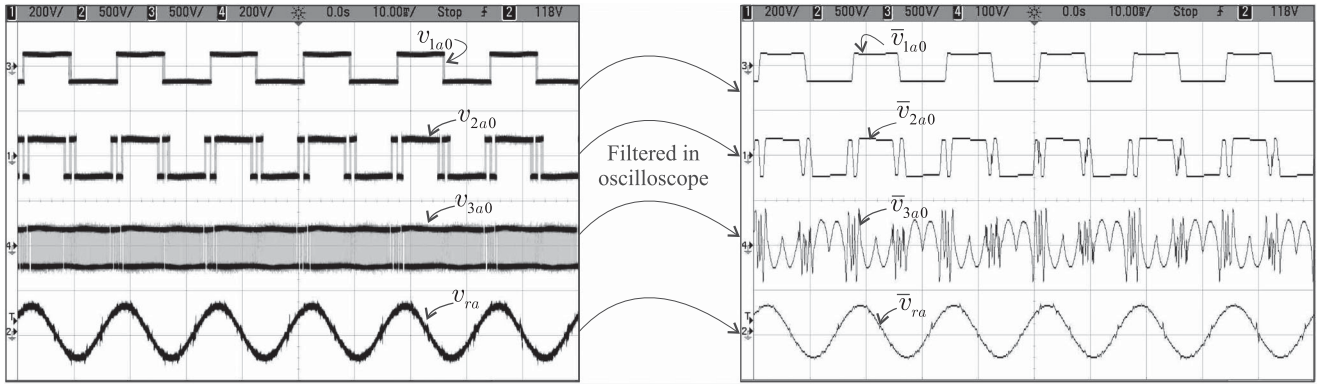

Fig. 14. PWM converter voltages in phase a. The PWM implementation of proposed MSC uses three converters (1, 2, and 3) and three transformers per phase with $N_1 = 1$, $N_2 = 2$, and $N_3 = 4$.

Fig. 13 shows the PWM implementation with proposed MSC having two single-phase transformers per phase (as a consequence it used converters 1 and 2). In such outcome, the transformers turns ratios were considered as $N_1 = 1$ and $N_2 = 2$. Notice that this result was similar to the one obtained in simulation, see Fig. 8(b). In addition, the converter 1 (with $N_1 = 1$) was clamped most of the time (i.e., it switched 1/3 of the operation cycle) while converter 2 (with $N_2 = 2$) switched over all operation cycle. This is an important characteristic because the converter 1 can provide lower switching losses in comparison with converter 2. Hence, converter 1 can be implemented with lower rated frequency switches.

Fig. 14, in turn, shows similar result where MSC operated with three single-phase transformers per phase (e.g., using converters 1, 2, and 3). The transformer turns ratios in this result were $N_1 = 1$, $N_2 = 2$, and $N_3 = 4$. The converter 1 (with $N_1 = 1$) provided the lowest switching frequency if compared to converters 2 and 3. The second converter that provided lowest switching was the converter 2 (with $N_2 = 2$). Finally, the converter 3 (with $N_3 = 4$) was the only one that switched over all the time.

VIII. Conclusion

This paper has presented a MSC based on cascaded transformers coupled with TPB converters. A generalization with K-stages was introduced in order to show that by increasing the number of cells, the performance can be improved as well as can increase the power rating of the compensator. The solution is an attractive option because it does not need any additional dc-link capacitors as observed in some conventional multilevel compensator, such as NPC [19], flying capacitors [21], cascaded HB [22], etc.

Since TPB modules are available in the market, the modularity is a good feature for this topology. The proposed MSC has two options of operation: 1) as a DVR; or 2) as a harmonic series active power filter (Series-APF). Some analysis and comparisons considering WTHD, semiconductor losses estimation and number of levels generated per power switches were presented. Compared with conventional HB, the proposed MSC has presented better values for these figures of merit. Simulation and experimental results were presented in order to validate theoretical considerations.

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